



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/255,777	02/23/99	YAMAZAKI	0756-1936

MMC1/0206
SIXBEY FRIEDMAN LEEDOM & FERGUSON PC
8180 GREENSBORO DRIVE
SUITE 800
MCLEAN VA 22102

EXAMINER
BOOTH, R

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 02/06/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.

09/255,777

Applicant(s)

YAMAZAKI ET AL.7

Examiner

Richard A. Booth

Art Unit

2812

-- Th MAILING DATE of this communication appears on the cover sheet with the corresponding address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 January 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19, 21-24, and 26-64 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-19, 21-24, and 26-64 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

- 15) ☐ Notice of References Cited (PTO-892)
- 16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 8/4
- 18) ☐ Interview Summary (PTO-413) Paper No(s) _____
- 19) ☐ Notice of Informal Patent Application (PTO-152)
- 20) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3, 5-9, 11-15, 17, 23-24, 26, 28-31, 33-39, 41-46, 48-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang, U.S. Patent 5,064,775 in view of Wolf et al., "Silicon Processing for the VLSI Era Volume 1: Process Technology", pages 175-180 and 323-325.

Chang shows the invention substantially as claimed including forming an amorphous or polysilicon semiconductor layer 34 on an insulating surface 32 with a thickness, for example, of one thousand angstroms (see column 4, lines 59-60); introducing boron 36 into the semiconductor layer so that the boron implanted region becomes at least a part of a channel region (see Figure 2); forming a gate insulating film 40 on the semiconductor layer; forming a gate electrode 42 on said gate insulating film; and forming source and drain regions (46,48) by implanting boron ions 44 into the semiconductor layer using the gate electrode 42 as a self-aligning mask (see Figures 2-6 and column 4, line 55 – column 5, line 37).

Chang lacks anticipation of forming the film as amorphous silicon and converting to polysilicon and using a screen oxide to perform the initial implantation.

Art Unit: 2812

Wolf et al. discloses that commonly in order to reduce damage to the semiconductor surface, layers are deliberately added, for instance, silicon oxide layers with thicknesses ranging from 200-300 angstroms (see page 323, "Implanting Through Surface Layers"). In addition, Wolf et al. also discloses that silicon layers that are deposited in an amorphous state are smoother than as-deposited polysilicon layers, even if the amorphous layers are subsequently crystallized at higher temperatures (see last six lines of page 179). In view of these two teachings, it would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit the silicon layer in the primary reference of Chang as an amorphous layer and form a screen oxide also for the reasons given above.

Claims 4, 10, 16, 18-19, 21-22, 27, 32, 40, and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang in view of Wolf et al. as applied to claims 1-3, 5-9, 11-15, 17, 23-24, 26, 28-31, 33-39, 41-46, 48-61 above, and further in view of Han et al., U.S. Patent 4,599,118.

Both Chang and Wolf et al. are applied as above but lack anticipation of forming a gate electrode by wet etching.

Han et al. discloses forming a very lightly doped p-type substrate followed by forming a gate electrode with tapered sides (see Figures 4-7 and column 3, line 66 – column 4, line 61). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the gate electrode in the primary reference of Chang with tapered edges because this allows for more tailoring of the device to overcome short channel effects. Regarding the use of wet

Art Unit: 2812

etching, official notice is taken that it is well known in the art to produce a gate electrode having tapered edges using wet etching. Official notice was also taken in the previous office action in this regard.

Claims 63-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang, U.S. Patent 5,064,775 in view of Wolf et al., "Silicon Processing for the VLSI Era Volume 1: Process Technology", pages 175-180 and 323-325 as applied to claims 1-3, 5-9, 11-15, 17, 23-24, 26, 28-31, 33-39, 41-46, 48-61 above, and further in view of Chiyuukou, JP 02-224253, submitted by applicant.

Chang and Wolf are applied as above but lack anticipation of crystallizing said film through irradiation by a laser through an insulating film.

Chiyuukou discloses performing an irradiation of amorphous silicon using an excimer laser through an oxide film 3 in order to protect the surface (see abstract and Figures). Even though the prior art reference states using the oxide film as the gate insulating film, the examiner takes official notice that in many instances it is better to replace this film with a new film because the damage caused by the laser leads to an inefficient gate insulating structure. In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to irradiate through the screen layer taught by Wolf because this provides protection for the underlying silicon surface.

Claim 62 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang in view of Wolf et al. and further in view of Han et al., U.S. Patent 4,599,118 as applied

Art Unit: 2812

to claims 4, 10, 16, 18-19, 21-22, 27, 32, 40, and 47 above, and further in view of Chiyuukou, JP 02-224253, submitted by applicant.

Chang, Wolf, and Han are applied as above but lack anticipation of crystallizing said film through irradiation by a laser through an insulating film.

Chiyuukou discloses performing an irradiation of amorphous silicon using an excimer laser through an oxide film 3 in order to protect the surface (see abstract and Figures). Even though the prior art reference states using the oxide film as the gate insulating film, the examiner takes official notice that in many instances it is better to replace this film with a new film because the damage caused by the laser leads to an inefficient gate insulating structure. In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to irradiate through the screen layer taught by Wolf because this provides protection for the underlying silicon surface.

Response to Arguments

Applicant's arguments filed 1-25-01 have been fully considered but they are not persuasive. Applicant argues that there is no motivation to combine references. However, Wolf et al. clearly shows that screen layers are used to control junction depth and prevent unnecessary damage. Furthermore, screen layers are not integral parts of the device so they are removed after the process is completed.

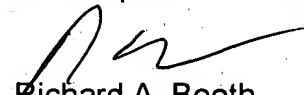
Art Unit: 2812

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard A. Booth whose telephone number is 308-3446. The examiner can normally be reached on Monday to Thursday from 7:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are 308-7724 for regular communications and 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 308-1782.


Richard A. Booth
Art Unit 2812